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A JOURNEY OF DISCOVERY

CRU Hardware Overview

ALICE Common Read-out Unit (CRU)

Engineering Design Review, CERN, 20 June, 2016

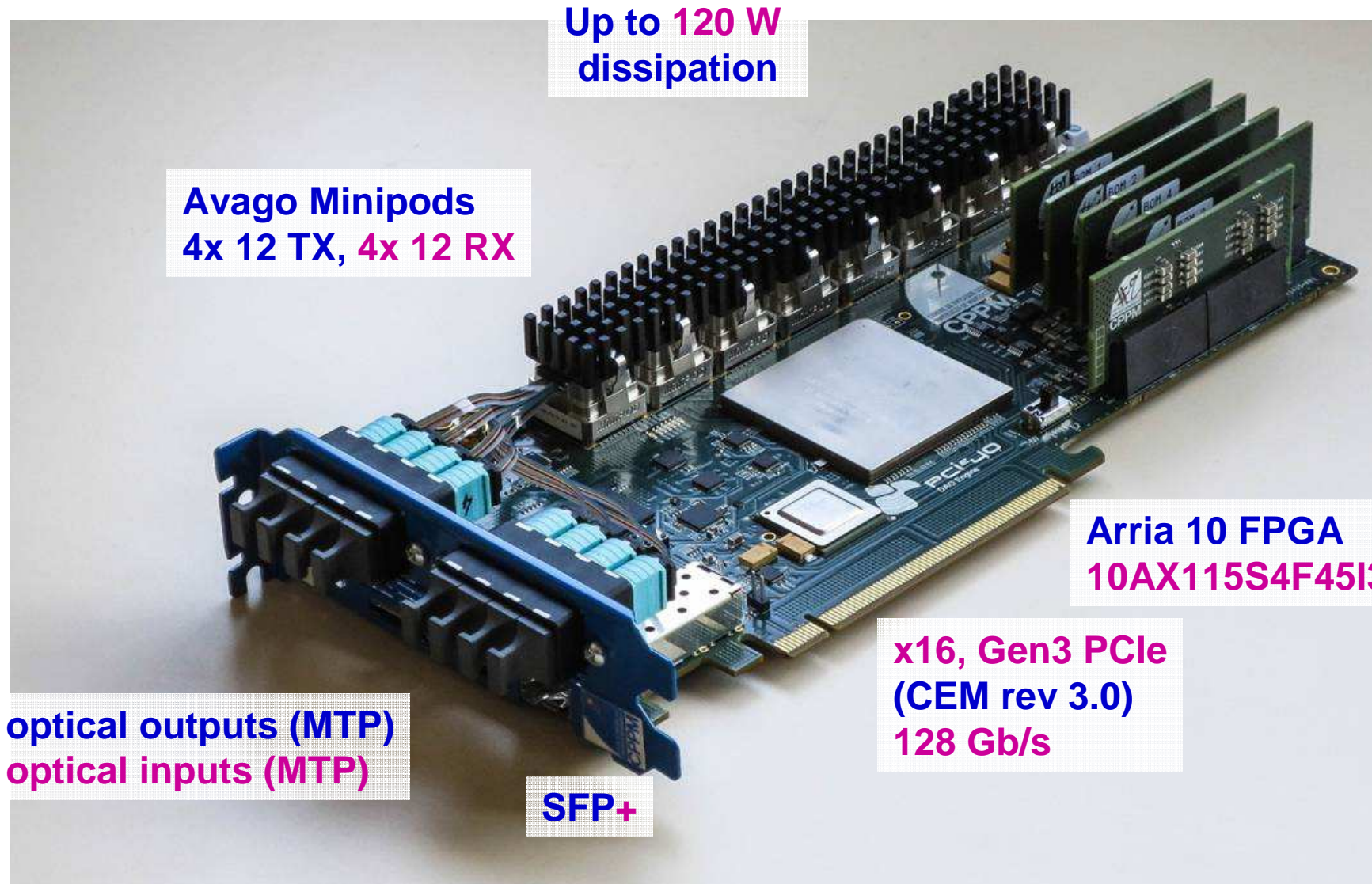
Tivadar KISS – Wigner RCP, Budapest

Jean-Pierre CACHEMICHE – CPPM, Marseille



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PCIe40 card of LHCb



Up to 120 W
dissipation

Avago Minipods
4x 12 TX, 4x 12 RX

Arria 10 FPGA
10AX115S4F45I3SG

48 optical outputs (MTP)
48 optical inputs (MTP)

x16, Gen3 PCIe
(CEM rev 3.0)
128 Gb/s

SFP+

CRU Hardware Development

- ALICE CRU HW: PCIe40 card developed by CPPM, Marseille fro LHCb
- Project leader: Jean-Pierre Cachemiche
- ALICE contributes to the prototypes testing and FW development with manpower

FPGA and boards Availability

- ALTERA delayed the launch of the final FPGA several times
 - We have ordered development boards for the central team with the final FPGA
 - We get two boards with ES3 on loan for 4 weeks /each
 - LHCb also delayed the productionm but started to do a test mounting of a few boards with ES3. We expect one board before the end of July and 4 more by mid September.

Prototypes testing and debugging

- Power regulator issues (regulators now on mezzanines) are debugged
- 2nd proto/first series still have an external PCIe bridge chip to merge the two x8 PCIe endpoints to a single edge connector
- Proper cooling is needed → not any server computers is acceptable



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Status

3. Board Design status

- First series production will start as soon as the final FPGA is available
- In the meantime, design of the final board will take place in Marseille from spring this year to autumn this year
- simplifications and optimizations of the board (e.g. omit power mezzanines, omit PCIe switch, other minor optimizations, however these means a major rerouting parts of the board)

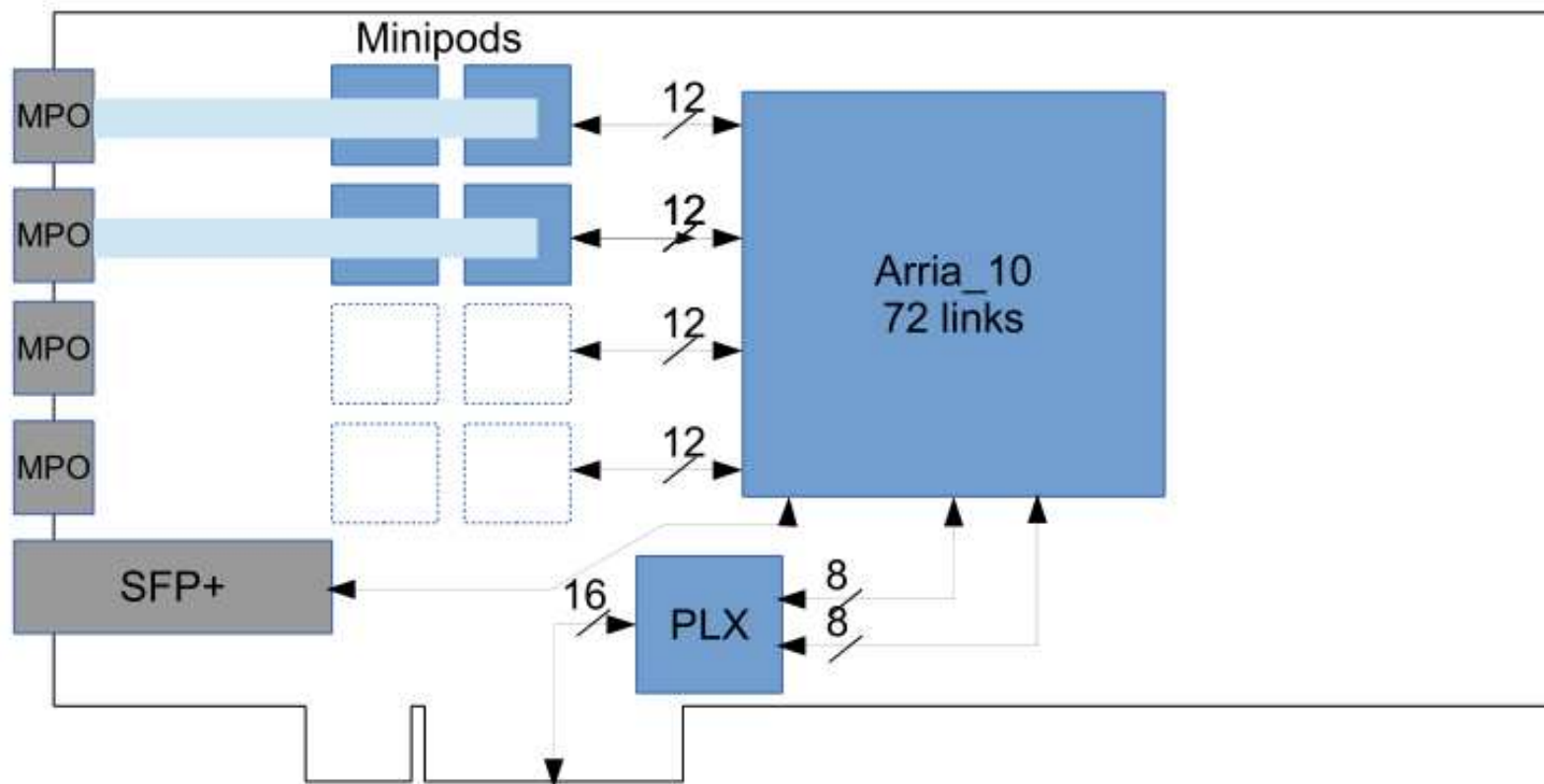
4. 2nd prototype/first series production in LHCb

- production of about 25 cards by CPPM includes 5 boards to ALICE CRU team and TPC
 - CERN DAQ group
 - Budapest group
 - Kolkata group
 - TPC / Heidelberg
 - TPC / Bergen
- Team account numbers collected and sent to CPPM
- CPPM strongly advises to use the already tested ASUS server computer
 - can be order from CPPM together with the PCIe40 cards or independently



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Block diagram of the PCIe40



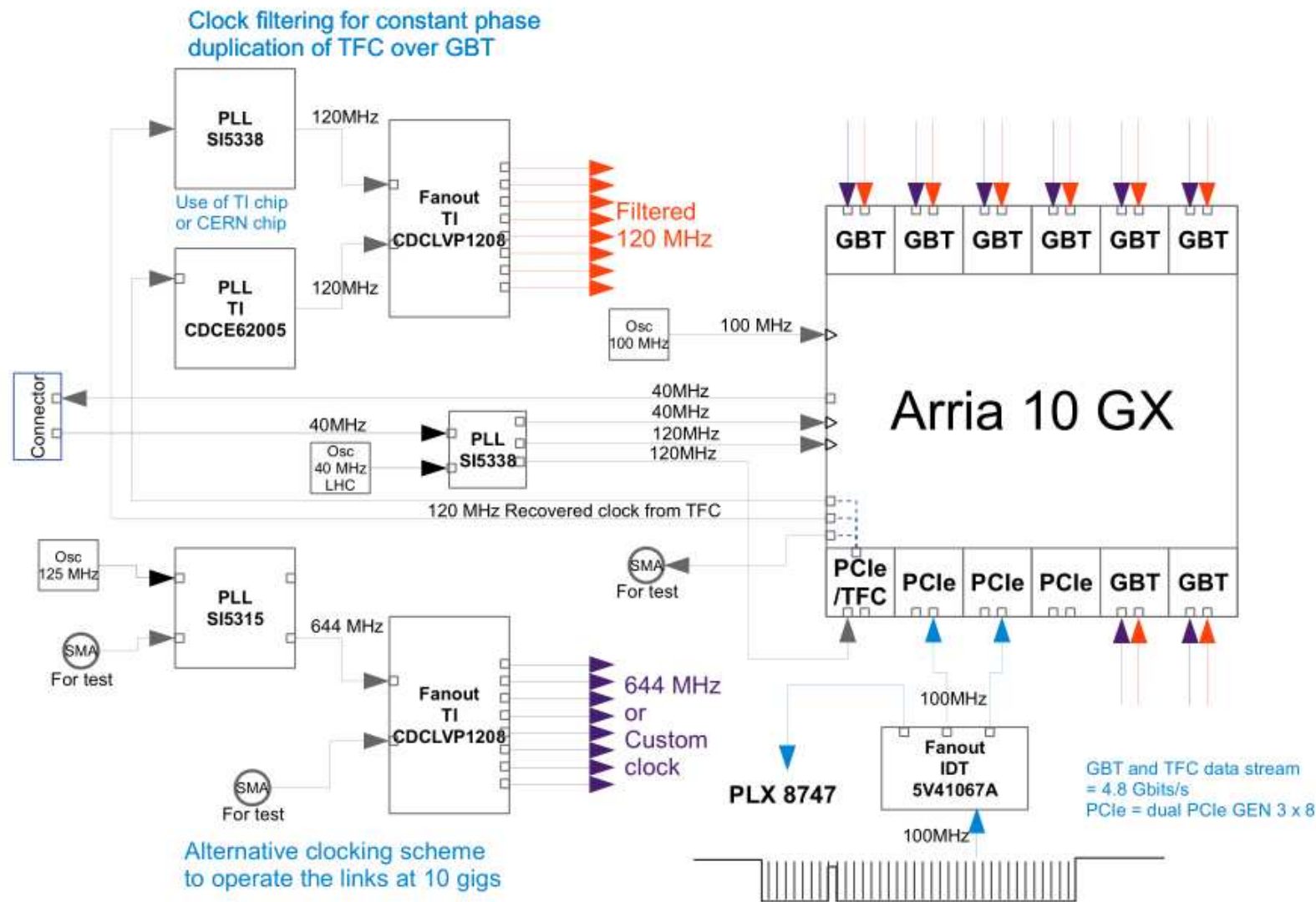
PCIe40_Specification_Draft0, rev1, LHCb Technical Note



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PCIe40 Clock Paths



PCIe40_Specification_Draft0, rev1, LHCb Technical Note

20.06.2016

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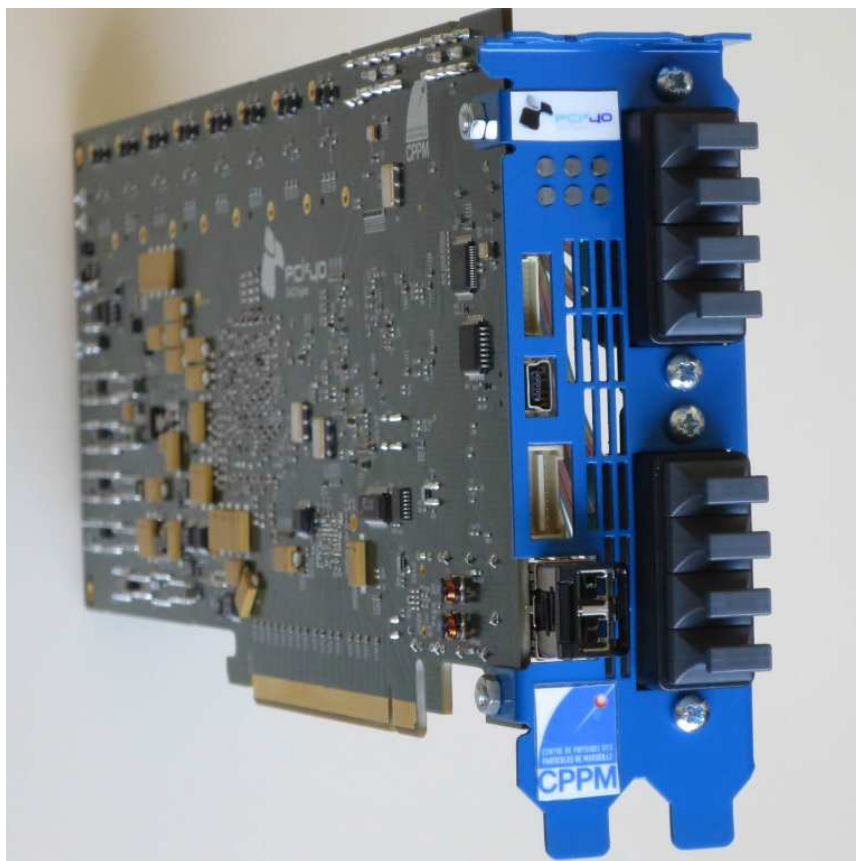
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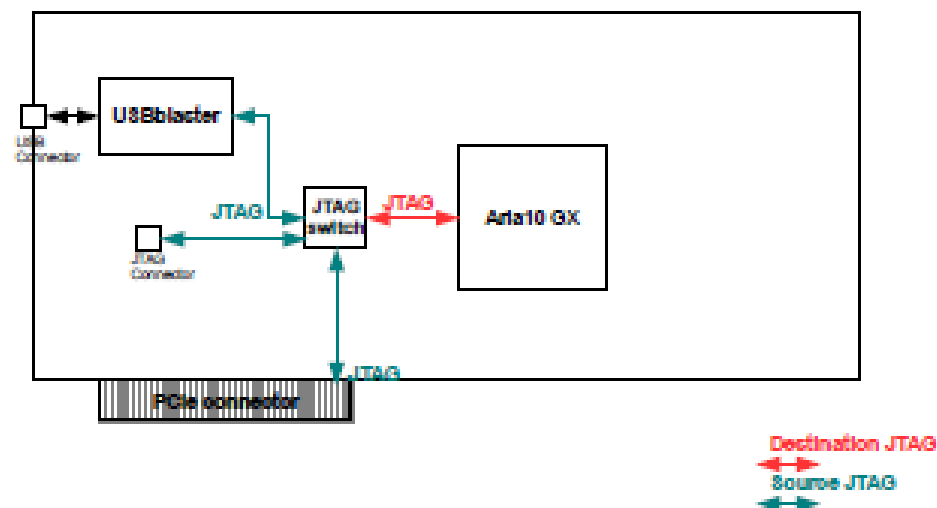
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Configuration, Front Panel Connectors

CRU front view



Configuration options



- JTAG programming through JTAG connectors
- On-board USB blaster
- Remote configuration from SW through the PCIe interface with CvP protocol



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Installation, Power, and Cooling

Installation, Power and Cooling

- Dual Slot card with Standard Height
- PCIe auxiliary power supply cable with 2x4 pin connector
- Dissipation up to 120 W
- Proper cooling is needed (to be finalized)
- Airflow of 2 m/s is required

Recommended Servers

- Developers strongly recommend to use a well tested, proven server machine for all users
- Recommended server: ASUS



PCIe40_Specification_Draft0, rev1, LHCb Technical Note